IEEE 3D System Integration Conference 2010 (3DIC)

Munich, November 16-18, 2010

Welcome from the Co-Chairs

The 2nd IEEE International 3D System Integration Conference (3DIC) is 2010 located at the Fraunhofer Society in Munich. It addresses engineers, scientists and entrepreneurs, who like to be informed about world-wide R&D activities, perspectives and challenges of 3D integration.

This conference combines the previous ASET and IEEE EDS Society sponsored International 3D System Integration Conference, held in Tokyo in 2007 & 2008 and the Fraunhofer and IEEE CPMT sponsored International 3D System Integration Workshop held in 2003 & 2007 in Munich. After the first combined conference in San Francisco 2009, the 2nd IEEE 3D System Integration Conference takes place in Munich in 2010, rotates to Tokyo in 2011 and returns to San Francisco in 2012.

3DIC 2010 will cover all 3D integration topics, including 3D process technology, materials, equipment, circuits technology, design methodology and applications.

The conference invites authors and attendees to interact with 3D researchers from all around the world. Purpose of this conference is creating a base for exchange of experience and to initiate an international technology platform to contribute essentially to the R&D in the area of system integration.

We are very proud that so many excellent speakers accepted to come and that we can offer a very sophisticated program on the tutorial day.

We hope you have an inspirational conference and enjoy your stay in Munich.

Welcome to the IEEE 3D System Integration Conference!

Dr. Peter Ramm
Head of Device and 3D Integration
Fraunhofer EMFT

Dr. Eric Beyne
Scientific Director of the Advanced Packaging and Interconnect Research
imec

Conference Day 1 - Tuesday, November 16th

Time	Programme
08:00 - 08:50	Welcome Coffee / Registration
08:50 - 09:00	Welcome in the Plenum Peter Ramm, Fraunhofer EMFT
09:00 - 09:40	Keynote: 3D Integration with TSV Interconnects: Technology Trends & Market Analysis Christophe Zinck, Yole Développement
09:40 - 10:20	Keynote: 3D Integration - A Server Perspective Jeff Burns, IBM
10:20 - 10:40	Coffee Break

Session 1: applications

Time	Programme
10:40 - 11:00	A 3D SoC Design for H.264 Application With On-Chip DRAM Stacking Tao Zhang, College of Engineering, Pennsylvania State University
11:00 - 11:20	Monolithic 3D Integration of SRAM and Image Sensor Using Two Layers of Single Grain Silicon Jaber Derakhshandeh, Delft Institute of Microsystems and Nanoelectronics
11:20 - 11:40	Application of the SLID-ICV Interconnection Technology for the ATLAS Pixel Upgrade at SLHC Ladislav Andricek, MPI Halbleiterlabor München
11:40 - 12:00	3D Stacked Buck Converter with 15-µm Thick Spiral Inductor on Silicon Interposer for Fine-Grain Power-Supply Voltage Control in SiP's K. Ishida, Institute of Industrial Science, The University of Tokyo

Time	Programme
12:00 - 13:30	Lunch
13:30 - 14:00	Invited - Samsung Challenges in TSV Commercialization Tae-Je Cho, Samsung Electron. Co. Ltd

Session 2: Technology 1

Time	Programme
14:00 - 14:20	Fabrication of TSV-Based 3D Silicon Interposers Dean Malta, Center for Materials & Electronic Technologies RTI International
14:20 - 14:40	High Performance 3D Interconnects Based on Electrochemical Etch and Liquid Metal Fill Harald Hedler, Siemens AG, Corporate Research and Technologies
14:40 - 15:00	All-Wet Fabrication Technology for High Aspect Ratio TSV Using Electroless Barrier and Seed Layers Fumihiro Inoue, Kansai University

Time	Programme
15:00 - 16:30	Coffee Break / Poster Session

Session 3a: Design

Time	Programme
16:30 - 16:50	Logic-on-Logic 3D Integration and Placement Thorlindur Thorolfsson, North Carolina State University
16:50 - 17:10	Design and Timing Optimization of a 3D Stacked Multi-Core Microprocessor Young-Joon Lee, Georgia Institute of Technology
17:10 - 17:30	Hierarchical 3D Interconnection Architecture with Tightly-Coupled Processor-Memory Integration Ito Kiyoto, ASET
17:30 - 17:50	Thermal Isolation in 3D Chip Stacks Using Vacuum Gaps and Capacitance Isolation Paul D. Franzon, Rambus Inc., Chapel Hill, NC, and Los Altos, CA

Session 3b: Test

Time	Programme
17:50 - 18:10	3D DfT Architectures for Pre-Bond and Post-Bond Testing Erik Jan Marinissen, imec
18:10 - 18:30	Developing Digital Test Sequences for Through-Silicon Vias within3D Structures Matthias Gulbins, Fraunhofer Institut für Integrierte Schaltungen IIS Dresden

Time	Programme
18:30 - 19:30	End of Day 1, Time for change, Change Location
19:30	Evening Event, Augustiner Bräu

Conference Day 2 - Wednesday, November 17th

Time	Programme
08:30 - 09:00	Welcome Coffee / Registration for new arrivals
09:00 - 09:40	Keynote: 3D R&D Technology for the Future Voyage in Japan Kenzo Inagaki, ASET
09:40 - 10:20	Keynote: 3D Heterogeneous Integration for Novel Functionality Montserrat Fernandez-Bolanos, EPFL Europe
10:20 - 10:50	Coffee Break

Session 4: Techno

Time	Programme
10:50 - 11:10	Reliability Testing of High Aspect Ratio TSV Structures Jason Reed, RTI International / MCNC Campus
11:10 - 11:30	Impact of Micro-Joint Induced Stress in Thinned 3D-LSIs after Wafer Bonding M. Murugesan, NICHe, Tohoku University
11:30 - 11:50	Through Silicon Photonic Via (TSPV) with Si Core for Low Loss and High-Speed Data Transmission in Opto-Electronic 3D LSI Akihiro Noriki, Tohoku University
11:50 - 12:10	A Successful Implementation of Dual Damascene Architecture to Copper Rebha El Farhane

Time	Programme
12:10 - 13:50	Lunch
13:50 - 14:20	Invited - imec Cost Effectiveness of 3D Integration Options Dimitrios Velenis, imec

Session 5: Design exploration

Time	Programme
14:20 - 14:40	3D Architecture Exploration and PathFinding for Maximal IP Re-Use Lisa McIlrath, R3 Logic, Incorporated
14:40 - 15:00	Design and Early Performance Evaluation of 3-D Stacked Chip Multi-Vector Ryusuke Egawa, Tohoku University
15:00 - 15:20	Enabling Power Distribution Network Analysis Flows for 3DICs Xiang Hu, Department of Electrical and Computer Engineering University of California

Time	Programme
15:20 - 17:00	Coffee Break / Poster Session
17:00 - 17:30	Invited - NTU Fine-Pitch Bump-less Cu-Cu Bonding for Wafer-on-Wafer Stacking and Its Quality Enhancement Chuan Sen Tang, NTU, Singapore

Session 6: Stacking

Time	Programme
17:30 - 17:50	Evaluation of Alignment Accuracy on Chip-to-Wafer Self-Assembly and Mechanism on the Direct Chip Bonding at Room Temperature Takafumi Fukushima, Tohoku University
17:50 - 18:10	Post-Bond Sub-500 nm Alignment in 300 mm Integrated Face-To-Face Wafer-To-Wafer Cu-Cu Weng Hong Teh, 3D Interconnects TD, Intel Assignee to SEMATECH

Time	Programme
18:10	End of Day 2

Conference Day 3 / Tutorial Day, Thursday, November 18th

08:00 - 08:30 Welcome Coffee and Registration

08:30 - 10:00 Special Session FREE ATTENDANCE
3DIC Multi-Project Fabrication Run being organized by CMC Microsystems, CMP, MOSIS, and Tezzaron
Bernard Courtois, CMP
Vance Tyree, MOSIS
Kholdoun Torki, CMP
Paul D. Franzon, NCSU
Gregory Deptuch, FERMILAB
Valerio Re, Univ. Bergamo
Jean-Claude Clemens, CPPM
Marc-André Tetrault, Univ. Sherbrooke
Ian McWalter, CMC

10:00 - 10:15 Coffee Break

10:15 - 12:15 Tutorial 1 - Part 1
3DIC Design
Paul D. Franzon, NCSU Raleigh NC
Erik Jan, Marinissen, IMEC vzw, Leuven

12:15 - 12:30 Break in the room

12:30 - 13:30 Tutorial 1 - Part 2
Test of 3D-SICS
Paul D. Franzon, NCSU Raleigh NC
Erik Jan, Marinissen, IMEC vzw, Leuven

13:30 - 14:30 Lunch

14:30 - 16:30 Tutorial 2 - Part 1
Thin Wafer Processing and Electrostatic Carrier Technology
Ira Balaj, Protec Carrier Systems
Christof Landesberger, Fraunhofer EMFT, Munich

16:30 - 16:45 Break in the room

16:45 - 17:45 Tutorial 2 - Part 2
Thin Wafer Processing and Electrostatic Carrier Technology
Ira Balaj, Protec Carrier Systems
Christof Landesberger, Fraunhofer EMFT, Munich

17:45 End of Tutorial Day

3D Architecures and applications

P3 A Block-Parallel Signal Processing System for CMOS Image Sensor with Three-Dimensional Structure
Koji Kiyoyama, Nagasaki Instituted of Applied Science

P11 CMIT- A Novel Cluster-based Topology for 3D Stacked Architectures
Masoud Daneshtalab, University of Turku

P13 Cache Partitioning Strategies for 3-D Stacked Vector Processors
Yusuke Funaya, Graduate School of Information Sciences Tohoku University

P18 Development of a CAD Tool for 3D-FPGAs
Naoto Miyamoto, Tohoku University

P35 Solution Space Investigation and Comparison of Modern Data Structures for Heterogeneous 3D Designs
Robert Fischbach, TU Dresden, Institut fuer Feinwerktechnik und Elektronik-Design (IFTE)

P5 Pixel Detectors in 3D Technologies for High Energy Physics
Grzegorz Deptuch, Fermi National Accelerator Laboratory

P23 In-Pixel ADC for a Vision Architecture on CMOS-3D Technology
Manuel Suárez, University of Santiago de Compostela

P25 3D Memory Stacking for Fast CheckpointingRestore Applications
Jing Xie, Pennsylvania State University

P1 Real-time Thermal Management of 3D Multi-core System with Fine-grained Cooling Control
Hao Yu, Nanyang Technological University, School of Electrical and Electronic Engineering

P24 Performance Analysis of 3-D Monolithic Integrated Circuits
Shashi-Kanth Bobba, Integrated Systems Laboratory, EPFL

P36 3DIC Design and Implementation – A Challenge for Engineers or Corporate Management
Herb Reiter, eda 2 asic Consulting

Through Si via technology and wafer thinning for 3D integration

P4 A Novel Concept for Ultra-Low Capacitance Via-Last TSV
Yann Civale, IMEC

P17 TSV Development for Miniaturized MEMS Acceleration Switch
Nicolas Lietaer, SINTEF ICT Microsystems and Nanotechnology

P28 Silicon-Interposer with High Density Cu-filled TSVs
Robert Wieland, Fraunhofer EMFT

P27 300mm Wafer Thinning and Backside Passivation Compatibility with Temporary Wafer Bonding for 3D Stacked IC Applications
Anne Jourdain, IMEC

P29 Development of High Accuracy Wafer Thinning
Chuichi Miyazaki, ASET

3D stacking of devices

P30 Low Temperature Direct Wafer to Wafer Bonding for 3D Integration
Gweltaz Gaudin, SOITEC SA -Parc Technologique des Fontaines

P14 Recent Developments of Cu-Cu Non-thermo Compression Bonding for Wafer-to-Wafer 3D Stacking
Ionut Radu, SOITEC S.A. - Parc Technologique des Fontaines

P2 Wafer-Level Hybrid Bonding Technology with Copper/Polymer Co-planarization
Aoki Mayu, ASET (Hitachi)

P20 High Density 3D Integration by Pre-applied Inter Chip Fill
Akihiro Horibe, ASET

P22 Wafer-Level Three-Dimensional Integration Using Hybrid Bonding
Kuan-Neng Chen, National Chiao Tung University

P31 Use of Optical Metrology Techniques for Monitoring of CMOS Sensor Wafer Level Packaging Processes
Delphine Le Cunff, ST Microelectronics

P6 Pre Bonding Metrology Solutions for 3D Integration
Gregory Riou, SOITEC SA -Parc Technologique des Fontaines

Performance of 3D stacks

P15 Wireless Power Transfer Using Resonant Inductive Coupling for 3D Integrated ICs
Sangwook Han, University of Michigan

P16 A High-Speed, Low-Power Capacitive-Coupling Transceiver for Wireless Wafer-Level Testing Systems
Kim Gil-Su, Institute of Industrial Science, University of Tokyo

P19 3D System on Chip Memory Interface Based on Modelled Capacitive Coupling Interconnections
Mauro Scandiuzzo, ST Lab - ARCES (Advanced Research Center on Electronic Systems "E.De Castro")

P37 Crosstalk Evaluation, Suppression and Modeling in 3D Through-Strata-Via (TSV) Network
Zheng Xu, Rensselaer Polytechnic Institute

P21 A Study of IR-drop Noise Issues in 3D ICs with Through-Silicon-Vias
Moongon Jung, Georgia Institute of Technology

P26 Early Estimation of TSV Area for Power Delivery in 3D Integrated Circuits
Naumann H. Khan, Department of Computer Science Tufts University

P34 Power Delivery Network Design and Optimization for 3D Stacked Die Designs
Pratyush Singh, Apache Design Solutions Inc.

P33 Integration of Multi Physics Modeling of 3D Stacks into Modern 3D Data Structures
Peter Schneider, Fraunhofer Institute for Integrated Circuits Design Automation Division, Dresden

P40 Additive TSV/Interconnect Fabrication
Gerrit Oosterhuis, TNO Science and Industry

Conference Venue, 3DIC Conference, November 16th-17th

"Fraunhofer Haus"
Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V.

Hansastraße 27c • 80686 Munich • Phone +49 89 1205 0

Tutorial Day, November 18th

Fraunhofer-Einrichtung für Modulare Festkörper-Technologien EMFT

Hansastraße 27d • 80686 Munich • Phone +49 89 54759 0

Recommended Conference Hotel

Sheraton Hotel Munich Westpark

Garmischer Straße 2 • 80339 Munich • Phone +49 89 5196 0

Dinner Location November 16th

Augustiner Keller München

Arnulfstraße 52 • 80335 München • Phone +49 89 5943 93

How to reach

Please note that at all locations there are very limited parking spaces. We therefore strongly recommend to use public transportation.

"Fraunhofer Haus"

Take 'U-Bahn' U4 or U5, direction to 'Laimer Platz', exit at 'Heimeranplatz'. Follow the signs to "Hansastrasse", turn left and register at the front desk in "Fraunhofer Haus" at Hansastraße 27c.

Fraunhofer EMFT

There is no direct access to Fraunhofer EMFT, please register at the front desk at the "Fraunhofer Haus"

The Sheraton Hotel Munich Westpark

The hotel is in walking distance to the Fraunhofer Haus directly at the U/S-Bahn station Heimeranplatz.

Augustiner Keller

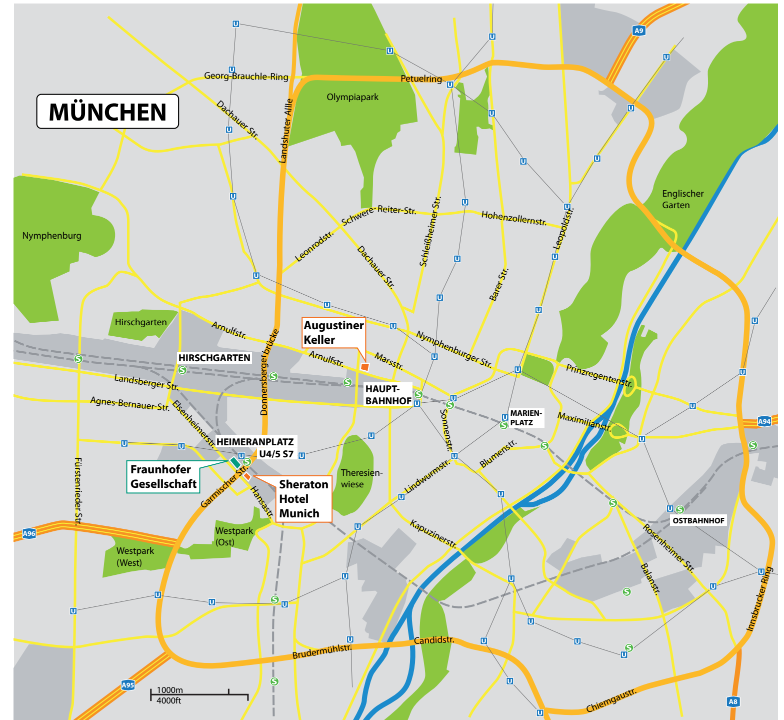
From Fraunhofer Haus and the Sheraton hotel you can walk to the U/S-Bahn station Heimeranplatz.

Take either
U5 (direction Neuperlach Süd) or U4 (direction Arabellapark) exit Hauptbahnhof (main station) or S7 (direction Kreuzstrasse) exit Hackerbrücke or Hauptbahnhof.

From Hackerbrücke or Hauptbahnhof it is only a short walk to the Augustiner Keller.

U/S-Bahn Departure Times Heimeranplatz

S7 (6 min. to Hackerbrücke): 18:40, 19:00, 19:20
U5 / U4 (4 min. to Hauptbahnhof): every 5 min.



Munich's claim to being the 'secret capital' of Germany is alive and well. With 1.3 million inhabitants Munich is the biggest city of Bavaria and the third biggest city of Germany.

More than 70 million people from all over the world visit the Bavarian capital each year. Munich's parks, stunning architecture, history, culture, beer gardens and a magnificent countryside give it a very special character and are the reason why so many people decide to visit the city on the Isar River.

Pulsing with prosperity and cosiness, Munich revels in its own contradictions. Folklore and age-old traditions exist side by side with sleek BMWs, designer boutiques, high-powered industry and distinguished research institutions.

Its museums include world-class collections of artistic masterpieces, and it offers exceptional music and cultural scenes.

Despite all its sophistication, Munich retains a touch of provincialism that visitors find charming. The people's attitude is one of live-and-let-live – and the Müncheners will be the first to admit that their 'metropolis' is little more than a world village. During Oktoberfest representatives of the entire planet can be found at the Theresienwiese.

Beside other attractions, no visit to Munich would be complete without a visit to one of its numerous beer halls or beer gardens.

We wish you a pleasant stay!

Your Conference Guide contains:

Welcome Note from the Co-Chairs
Agenda Conference Day 1, Day 2, Day 3 / Tutorial Day
Poster Session Overview
Locations/How to reach
Destination Outline Munich

Important phone numbers

Ambulance 19222
Doctor 112
Police 110

Munich airport information +49 89 975 00
Taxi Munich +49 89 450 54 200
Airport Transfer +49 89 450 54 400

Event Manager
Bärbel van Essen
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